Output Buffer with Low-Voltage Devices to Driver High-Voltage Signals for PCI-X Applications

ABSTRACT

An output buffer circuit with low-voltage devices to driver high-voltage signals for PCI-X applications is proposed. Because power supply voltage of PCI-X is at 3.3V, the high-voltage gate-oxide stress is a serious problem to design PCI-X I/O circuit in a 0.13 μm 1V/2.5V CMOS process with only low-voltage gate oxide. This proposed output buffer circuit can be operated at 133 MHz in 3.3V PCI-X environment without causing high-voltage gate-oxide reliability problem. In this design, the circuit is implemented in a 0.13 μm 1V/2.5V CMOS process and the output signal swing can be 3.3V. Besides, a level converter that converts 0V~1V voltage swing to 1V~3.3V voltage swing is also presented.